IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/729,331	§		
Filed: December 05, 2003	§	Examiner:	Fennema, Robert E.
Inventors:	§	Group/Art Unit:	2183
Teik-Chung Tan	§	Atty. Dkt. No:	5500-91700
Gregory William Smaus	§		
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Title: Multiple Control Sequences per Row of Microcode ROM	§		

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reasons stated below.

Claims 1-27 are pending in the application. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims and several of the dependent claims are presented. Applicants assert that numerous other ones of the dependent claims also recite distinctions over the cited art and that additional arguments, e.g., directed to the subject matter of others of the dependent claims, will be presented if and when the case proceeds to Appeal.

The Examiner rejected claims 1-3, 5-10, 12-14, 16-21, 23, 24 and 27 under 35 U.S.C. § 102(b) as being anticipated by Tredennick et al. (U.S. Patent 4,338,661) (hereinafter "Tredennick"). Applicants respectfully traverse this rejection for at least the following reasons.

Regarding claim 1, in the Advisory Action, the Examiner submits that Tredennick teaches *wherein a row in the microcode ROM stores a plurality of groups of microcode operations*, using an example in which one row in the nano control of Tredennick includes four nanowords: swap1, swap2, tasm1, and tasm2. The Examiner interprets this example as teaching a plurality of groups of microcode operations (swap and tasm, each with two parts). The Examiner further asserts, "the groups could contain a single instruction, with some rows containing up to 4 groups of operation, based on the particular row and exact length of ROM chosen to implement the design." However, a single instruction is not "a group of microcode operations (plural) … comprised in a microcode routine" as recited in claim 1, and having the additional limitations of claim 1 discussed below. The plain wording of claim 1 requires that the group referred to in subsequent limitations contain multiple operations. For example, claim 1 recites, in part, "wherein in response to accessing the group of microcode operations comprised in the microcode routine..." and later, "the control sequence associated with the group of microcode operations…" These limitations are clearly not anticipated by a group containing only one microcode operation, as the Examiner suggests.

Applicants also assert that Tredennick fails to teach or suggest *wherein the row stores an associated control sequence for each of the plurality of groups of microcode operations*. The Examiner cites column 15, lines 52-55 and 59-66 as teaching this limitation. These passages describe two formats for microwords. In a microword of a conditional branch type (type II), bits 7 thru 14 comprise a next micro ROM base address (NMBA) for the micro and nano control stores, and are augmented by 2 additional bits supplied by branch control logic (C0 and C1) in order to specify the next address for the control stores (i.e., in order to select a single word line for the micro and

nano control stores). In microwords having format type I, bits 2 and 3 comprise a type field (TY) which specifies the source of the next address for the control stores as being from one of the 3 possible addresses provided by the instruction register sequence decoder or from a direct branch address provided by bits 5 thru 14 of the microword. Thus, these passages disclose that information stored in each microword may be used in determining the next address used to select a single word line (and, therefore, a single next operation) for each of the control stores. They clearly do not describe a control sequence being **associated with a group of multiple instructions** comprised in a row in the microcode, as in Applicants' claimed invention. There is nothing in these passages or elsewhere that teaches or discloses a row storing an associated control sequence for each of the plurality of groups of microcode operations stored in the row. **Using the Examiner's example in the eighth row of FIG. 11A, there is no control sequence in Tredennick associated with a group of operations that includes swap1 and swap2, nor with a group of operations that includes tasm1 and tasm2.** Instead, each of the individual microwords corresponding to these nanowords includes a micro ROM base address for the next individual microword and nanoword to be accessed.

Further regarding claim 1, Tredennick fails to teach or suggest a control sequence logic unit coupled to the microcode ROM, wherein in response to accessing the group of microcode operations comprised in the microcode routine, the control sequence logic unit is configured to use the control sequence associated with the group of microcode operations to identify another row storing one or more next groups of microcode operations comprised in the microcode routine. The Examiner cited column 15, lines 37-40 as teaching this limitation ("it selects the next line of the ROM, which is output from the microcode ROMs as shown in column 15, lines 52-55 and 59-66.") First, as discussed above, Tredennick does not disclose a control sequence **associated with a group of microcode operations**. In addition, column 15, lines 37-40 merely describes that the micro ROM is addressed by the 10-bit output of address selection block 64. Furthermore, the Examiner's statement "it selects the next line of the ROM" has no basis in Tredennick. As discussed above, column 15, lines 52-55 and 59-66 describes how the next address to be decoded for the control stores is determined for microwords having type I and type II formats. None of these descriptions includes a control sequence identifying an other row storing one or more next groups of microcode operations comprised in the (same) microcode routine. Instead, for each individual operation, a next address is provided for a next individual operation. **Using the Examiner's example, there is clearly not a control sequence (or next micro ROM address) associated with a group of operations including swap1 and swap2 that identifies an other row storing one or more next groups of microcode operations comprised in the (same) microcode routine, as the "swap1" microcode routine includes only the two operations swap1 and swap2 on the eighth row of FIG. 11A (see Appendix A).** Similarly, there is clearly not a control sequence (or next micro ROM address) associated with a group of operations containing trap1 and trap2 that identifies an other row storing one or more next groups of microcode operations comprised in the (same) microcode routine, as the "trap1" microcode routine includes only the two operations trap1 and trap2 on the eighth row of FIG 11A (see Appendix A). Applicants assert that nothing in Tredennick teaches a control sequence associated with a group microcode operations comprised in a microcode routine that is used to identify an other row storing one or more next groups of microcode operations comprised in the (same) microcode routine, as required by claim 1.

For at least the reasons above, Applicants again assert that Tredennick clearly does not teach all of the limitations of Applicants' claim 1. Therefore, the rejection of claim 1 is unsupported by the cited art and removal thereof is respectfully requested. Claims 12 and 23 include limitations similar to claim 1, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 27, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *a microcode ROM, wherein a row in the microcode ROM stores a plurality of groups of microcode operations and wherein the row stores an associated control sequence for each of the plurality of groups.* In the previous Office Action, the Examiner again cited column 15, lines 33-34, 36-37, 52-55, and 59-66 as teaching these limitations. However, as discussed above regarding claim 1, Tredennick does not teach or suggest a row in the microcode storing groups of microcode operations and a control sequence associated with each of the groups.

Further regarding claim 27, Tredennick fails to teach or suggest *means for accessing a control sequence associated with one of the plurality of groups of microcode operations and responsively accessing a next group of microcode operations stored in the microcode ROM.* The Examiner again cited "Column 15, lines 37-40, it selects the next line of the ROM, which is output from the microcode ROMs as shown in column 15, lines 52-55 and 59-66." However, as discussed above regarding claim 1, Tredennick does not teach or suggest groups of microcode

operations stored in a row that also stores a control sequence associated with one of the groups of microcode operations, and therefore, cannot teach or suggest accessing such a control sequence or responsively accessing a next group of microcode operations stored in the microcode ROM. Therefore, Tredennick cannot be said to anticipate claim 27.

In the Response to Arguments section of the Final Action, the Examiner submits that claim 27, "has similar limitations, except the control addresses a group instead of a row, which is taught by Tredennick as explained above." Applicants assert that, as discussed above regarding claim 1 and claim 27, Tredennick does not teach a control sequence associated with each one of a plurality of groups of microcode operations, nor that such control sequences are stored in a row containing each of the plurality of groups of microcode operations, as required by claim 27. For at least the reasons above, the rejection of claim 27 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claim 3, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein the control sequence logic unit is configured to identify which of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine based on information contained in the control sequence associated with the group of microcode operations stored in the row*. The Examiner cited column 15, lines 52-55 and 59-66, "which defines which row and position the next group is located," as teaching these limitations. However, this citation does not teach identifying a row and position for a next group of microcode operations. Instead, this passage describes how the next address is determined for an individual microword having a type I or type II format. There is nothing in the Examiner's citation or elsewhere in Tredennick that teaches or suggests that identifying the next address (or "a row and position") has anything to do with identifying which of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the (same) microcode routine, as required by claim 3, only that it identifies a next (individual) operation.

In the Response to Arguments section of the Final Action, the Examiner submits, "The cited portion discloses that the address directs the processor to the next group in the routine, which must specify a row, as discussed in Claim 1. It can be further seen in Figure 11a that the 10-bit address does select a position using bits A1 and A0." Applicants again assert that the address selects a single microword or nanoword, not a group of microcode operations stored in a row and comprised in the microcode routine. For at least the reasons above, the rejection of claim 3 is unsupported by the cited art and removal thereof is respectfully requested. Claim 14 includes limitations similar to claim 3, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 5, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein if the group of microcode operations comprises at least one branch operation, the control sequence logic unit is configured to identify the next group of microcode operations in the microcode routine dependent on a branch prediction as well as the control sequence associated with the group of microcode operations*. The Examiner cited column 15, lines 49-55 ("teach a microcode instruction for branches") and column 17, lines 29-32 ("show that the outcome either way will be in the same row specified by the control sequence") as teaching these limitations. The Examiner's citation in column 17 states, "Thus, two microwords which serve as alternate destinations for a particular conditional branch type microword must be placed in the same logical row of the micro ROM." Applicants assert that this citation does not describe identifying the next group of microcode operations in a microcode routine, but instead describes two alternate (individual) addresses that may be the destination of a branch operation. Furthermore, the Examiner's remarks appear to teach away from identifying the next group of operations dependent on a branch prediction. Instead, they imply that no branch prediction is necessary (or performed) because "the outcome either way will be in the same row." **In fact, branch prediction is not disclosed in Tredennick.** Therefore, Tredennick clearly cannot be said to anticipate claim 5.

In the Response to Arguments section of the Final Action, the Examiner submitted, "Applicant has argued that Tredennick teaches away from the claims because both outcomes are located in the same row. However, Tredennick teaches this is done to minimize the size of storage, to prevent multiple instances of the branch from being put in memory (Column 2, Lines 40-50), and as explained above, Tredennick can specific positions inside a row, the fact that they are in the same row is space optimization." The Examiner has misunderstood Applicants' argument. Applicants' argument was that Tredennick taught away from this limitation for several reasons. One is that all of the possible next microwords to be accessed will be in the same row, therefore the next row to be accessed is already known. The fact that the outcomes are positioned in the same row to save space is irrelevant. The second

is that no branch prediction is described, as required by Applicants' claim. In addition, Tredennick does not teach identifying a row containing a next **group** of microcode operations comprised in the microcode routine, as required by Applicants' claim, only a next individual microword (and/or nanoword). For at least the reasons above, the rejection of claim 5 is unsupported by the cited art and removal thereof is respectfully requested. Claims 16 and 24 include limitations similar to claim 5, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 6, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein the microcode ROM is divided into a plurality of segments, wherein a same number of groups of microcode operations is stored in each row of a given one of the plurality of segments, and wherein each row in the given one of the plurality of segments stores a different number of groups of microcode operations than each row in each other one of the plurality of segments*. The Examiner cited column 19, lines 22-27 as teaching this limitation ("for each row, the address may represent one, two, four, or up to eight different groups. So there are segments in the sense that some lines can contain a different number of groups than the other lines.") The Examiner has misquoted column 19. The Examiner's citation states, "Each word line in the micro ROM is represented by only one input address. Each word line in the nano ROM however may represent one, two, or four possible different input addresses. In the preferred embodiment of the data processor, a word line in the nano ROM may represent as many as eight different input addresses." However, "a word line" in Tredennick is not a row in the microcode ROM that stores a plurality of groups of microcode operations, as in Applicants' claimed invention. Instead, "a word line" selects a single microword and/or a single nanoword from the micro ROM and nano ROM, respectively. (See, e.g., column 19, lines 13-22: "the same address is presented to the decoders of both the micro ROM and the nano ROM. For any input address, there will be no more than one word line in each ROM which remains high. The line which remains high will cause the appropriate output value to be generated as the micro ROM output word and the nano ROM output word according to the coding at the intersection of the selected word line and the output columns." There is nothing in Tredennick that teaches or suggest the microcode ROM is divided into a plurality of segments having the limitations recited in claim 6 ("wherein a same number of groups of microcode operations is stored in each row of a given one of the plurality of segments, and wherein each row in the given one of the plurality of segments stores a different number of groups of microcode operations than each row in each other one of the plurality of segments.") Therefore, Tredennick cannot be said to anticipate claim 6.

In the Response to Arguments section of the Final Action, the Examiner submitted that "in Tredennick, the word line in one ROM is a row (the micro ROM), or a "group" in the nano ROM. Thus, when reading Tredennick as it was intended, a "row" or "word" in the micro ROM corresponds to multiple "words" in the nano ROM." **The Examiner is incorrect**. Tredennick teaches that one input address may be used to identify one word (which is not a "row" as defined by Applicants' claims) in the micro ROM and one word in the nano ROM. The mapping of multiple nano words to one micro word described by the Examiner is incorrect. Instead Tredennick teaches that more than one input address may identify the same nano word, as in the example detailed in the previous Response. For at least the reasons above, the rejection of claim 6 is unsupported by the cited art and removal thereof is respectfully requested. Claim 17 includes limitations similar to claim 6, and so the arguments presented above apply with equal force to this claim, as well.

Similarly, Tredennick fails to teach or suggest the limitations of claims 7-9. The Examiner cited column 19, lines 22-27 as teaching these limitations by the same reasoning applied to his rejection of claim 6. However, as discussed above, this citation has nothing to do with a plurality of segments in a microcode ROM, much less with such segments having the limitations recited in claims 7-9. As discussed above regarding claims 1 and 6, Tredennick clearly does not teach anything about segments of microcode operations defined or stored as in Applicants' claimed invention. Furthermore, Applicants again assert that Tredennick teaches nothing about the maximum width of any such segments or what would be stored in such a segment (e.g., *one group of microcode operations and one associated control sequence per row*, as claimed.) Therefore, Tredennick cannot be said to anticipate these claims. For at least the reasons above, the rejection of claims 7-9 is unsupported by the cited art and removal thereof is respectfully requested. Claims 18-20 include limitations similar to claims 7-9 and so the arguments presented above apply with equal force to these claims, as well.

In light of the foregoing remarks, Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested. If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are

due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5500-91700/RCK.

Also enclosed herewith are the following items:
☒ Notice of Appeal

Respectfully submitted,

/Robert C. Kowert/
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